REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on July 15, 2003, and the references cited therewith. No claims are amended, canceled, or added; as a result, claims 1-21 remain pending in this application.

'103 Rejection of the Claims

Claims 1-2, 4-5 and 7-8 were rejected under 35 USC ' 103(a) as being unpatentable over Gilbert et al. (U.S. 6,041,376) in view of Arimilli et al. (U.S. 6,138,218).

Claims 3, 6 and 9 were rejected under 35 USC ' 103(a) as being unpatentable over Gilbert et al. in view of Arimilli et al. and Donley et al. (U.S. 5,761,446).

Claims 10-21 were rejected under 35 USC ' 103(a) as being unpatentable over Vogt et al. (U.S. 5,897,656) in view of Gilbert et al.

The pending claims are directed to prevention of live-lock in a multi-processor system. As stated in the Background section of the present application:

> "However, certain architectures do not permit multiple bus transactions to be outstanding for a single shared resource. In these architectures, the processor that initiated the transaction "first" is allowed to complete the transaction. All subsequent transactions are retried if the transactions are for the same resource and the transactions occur before the first transaction has completed. A transaction may be retried any number of times until the transaction is allowed to complete. However, a problem arises when one processor is "locked out" because it is always being retried.
>
> For example, such a problem can occur when multiple processors initiate bus transactions for the same resource at about the same time and the first processor that is granted the resource is only reading the resource. *In this case, a live-lock situation can occur if a subsequent bus transaction for the same resource is to modify the resource and that subsequent bus transaction is continually retried.* Even though the subsequent bus transaction to modify the resource is retried, the other processors still snoop the subsequent bus transaction. The first processor's cache memory contains a copy of the resource as a result of the read operation. However, the first processor's copy of the resource is then invalidated when the first processor snoops the subsequent bus transaction to modify the resource. This causes the first processor to issue another bus transaction to acquire a valid copy of the same resource. Live-lock occurs when the first processor that is just reading the resource is always being granted the

resource and a second processor that is trying to modify the resource is continually being retried."

The Applicant's invention as claimed addresses the problem of live-lock by identifying a first bus transaction the attempts to *modify* a shared resource and setting a status bit. Each subsequent *nonmodifying* bus transaction for the shared resource is retried until the status bit is cleared. Applicant respectfully submits that the Office Action did not make out a *prima facie* case of obviousness for the invention as claimed.

First, even if combined, the cited references fail to teach or suggest all of the elements of applicant's claimed invention. Independent claims 1, 7, 10, 15, and 17 recite the following elements that are not taught by the cited references.

- Independent claim 1 includes the following elements: "setting a status bit to indicate that a bus transaction attempting to *modify* the shared resource is pending; and retrying each subsequent *nonmodifying* bus transaction for the shared resource until the status bit is cleared."
- Independent claim 7 includes the following elements: "setting a status bit to indicate that a bus transaction attempting to *modify* the cache line is pending; issuing a second bus transaction to *read* the cache line; retrying the second bus transaction if the status bit is set. . ."
- Independent claim 10 includes the following element: "a status indicator associated with each one of the plurality of buffers, the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to *modify* the shared resource and the bus transaction is retried.
- Independent claim 15 includes the following element: "a status indicator associated with each one of the plurality of buffers, the status indicator to indicate when a first one of the processors initiates a bus transaction attempting to *modify* the system memory and the bus transaction is retried."
- Independent claim 17 includes the following element: "a plurality of status indicators to indicate that one of the bus transactions attempting to *modify* one of the cache lines is retried, at least one of the status indicators associated with each one of the buffers."

In contrast, Gilbert describes:

> "*A multiprocessor system that assures forward progress of local processor requests for data by preventing other nodes from accessing the data until the processor request is satisfied.* In one aspect of the invention, the local processor requests data through a remote cache interconnect. The remote cache interconnect tells the local processor to retry its request for data at a later time, so that the remote cache interconnect has sufficient time to obtain the data from the system interconnect. When the remote cache interconnect receives the data from the system interconnect, a hold flag is set. ***Any** requests from other nodes for the data are rejected while the hold flag is set.* When the local processor issues a retry request, the data is delivered to the processor and the hold flag is cleared. Other nodes may then obtain control of the data." (*see Abstract of Gilbert; emphasis added)*

Gilbert does not teach or suggest identifying bus transactions that attempt to *modify* a shared resource (as recited in claims 1, 7, 10, 15 and 17) and then retrying each subsequent *nonmodifying* bus transaction (as recited in claims 1 and 7) because the hold flag taught by Gilbert is used to cause *any* requests from other nodes for the data to be rejected while the hold flag is set. Even when combined with Arimilli or Vogt, Gilbert stills fails to teach or suggest all of the elements of claim 1-21.

Second, the Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002). The Office Action stated:

> "It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide for the storage of the flag (i.e. maintaining he integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli."

The Office Action further stated:

> "It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Gilbert with Vogt because it would provide guaranteed forward progress of processor requests for data by preventing other processors from accessing data until the processor request is satisfied as taught by Gilbert."

These are mere conclusory statements of subjective belief, so Applicant respectfully submits that the Office Action has not provided objective evidence for a suggestion or motivation to combine the references.

Furthermore, Applicant does not admit that Gilbert and Arimilli references are prior art, and reserves the right to swear behind them at a later date. Nevertheless, Applicant respectfully submits that the claims are distinguishable over Gilbert and Arimilli for the reasons argued above.

Thus, Applicant respectfully submits that the Office Action did not make out a *prima facie* case of obviousness for the invention as claimed. Reconsideration and allowance of claims 1-21 is respectfully requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 20 day of August, 2004

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